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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,857	08/25/2000	Dean Nobunaga	400.002US01	5906

7590 06/04/2003

FOGG SLIFER & POLGLAZE P A
P O Box 581009
Minneapolis, MN 55458-1009

EXAMINER
CHANG, ERIC

ART UNIT	PAPER NUMBER
2185	4

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,857	NOBUNAGA ET AL.	
	Examiner	Art Unit	
	Eric Chang	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-24 are pending.

Drawings

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3, 5, 9, 11-12, and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,936,977 to Churchill, et al.

5. As to claim 1, Churchill discloses a timing circuit comprising:

[a] a programmable non-volatile fuse circuit [FIG. 9, element 904, and col. 12, lines 63-67]; and

[b] an adjustable delay element coupled to the programmable non-volatile fuse circuit, the delay element has a plurality of propagation times selectable in response to the non-volatile fuse circuit [FIG. 9, element 902, and col. 12, lines 63-67].

Churchill teaches an adjustable delay element that is controlled by a programmable decode logic [col. 14, lines 11-15] that determines the propagation time of a signal through said adjustable delay element.

6. As to claims 3 and 11, Churchill discloses the programmable non-volatile fuse circuit comprises a plurality of flash memory cells [col. 14, lines 44-49].

7. As to claims 5, 12, and 16, Churchill discloses the adjustable delay element comprises a plurality of capacitors selectively coupled to a propagation path [col. 13, lines 41-45].

8. As to claim 9, Churchill discloses the adjustable timing circuit comprising a programmable non-volatile fuse circuit that controls an adjustable delay element, substantially as claimed. Churchill further teaches that the adjustable timing circuit may be used to control access to an array of memory cells [col. 4, lines 6-30]. Therefore, Churchill teaches a memory device comprising both the memory and the adjustable timing circuit, substantially as claimed.

9. As to claim 15, Churchill discloses the adjustable timing circuit comprising a programmable non-volatile fuse circuit that controls an adjustable delay element, substantially as claimed. Because Churchill teaches the circuit, Churchill also teaches the method implemented by the circuit, substantially as claimed.

10. As to claim 17, Churchill discloses the programmable non-volatile fuse circuit comprises a plurality of floating gate transistors [col. 14, lines 44-49]. Churchill teaches that the programmable element may comprise any type of programmable element, such as an electrical fuse comprising a floating gate transistor.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2, 4, 6-8, 10, 13-14, and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,936,977 to Churchill, et al. in view of U.S. Patent 6,219,813 to Bishop, et al.

13. As to claims 2, 10, and 18, Churchill discloses the adjustable timing circuit comprising a programmable non-volatile fuse circuit that controls an adjustable delay element, substantially as claimed. Furthermore, Churchill teaches that the output from the programmable non-volatile fuse circuit may be sent to a multiplexor prior to being used to configure the adjustable delay element [FIG. 11B, elements 1117 and 1119, and col. 14, lines 15-25]. However, Churchill does not teach that the circuit further comprises a volatile latch coupled between the programmable non-volatile fuse circuit and the adjustable delay element.

Bishop teaches that an adjustable delay element may be controlled by output from configuration latches or multiplexors [FIG. 1, element 110 and 122, and col. 5, lines 7-11]. Bishop therefore teaches a circuit that controls the adjustable delay element, and that such a circuit may comprise either multiplexors, as taught by Churchill, or latches, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ configuration latches as taught by Bishop. One of ordinary skill in the art would have been motivated to do so that the configuration information from the programmable fuse circuit may be used to control the adjustable delay element.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of using a programmable delay system to adjust the timing of memory control signals. Moreover, the latch means taught by Bishop would improve the flexibility of Churchill because it allowed the configuration to be maintained to the adjustable delay circuit even if the fuse circuit were subsequently re-programmed.

14. As to claim 4, Churchill teaches all of the limitations of the claim but does not teach that the circuit further comprises a latch coupled to an output of the adjustable delay element.

Bishop teaches a latch coupled to an output of the adjustable delay element [FIG. 1, element 114].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the output latch as taught by Bishop. One of ordinary skill in

the art would have been motivated to do so that the output from the adjustable delay element may be compared with other outputs for testing purposes.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of using a programmable delay system to adjust the timing of memory control signals. Moreover, the latch means taught by Bishop would improve the utility of Churchill because comparing the output from the adjustable delay element with other outputs for testing purposes can result in improving the timing of the memory system [col. 5, lines 11-20].

15. As to claim 6, Churchill discloses a timing circuit comprising:

[a] a programmable non-volatile fuse circuit [FIG. 9, element 904, and col. 12, lines 63-67]; and

[b] a plurality of delay elements coupled to the volatile latch, comprising propagation paths, a plurality of capacitors selectively coupled to the propagation path selectable in response to the non-volatile fuse circuit [FIG. 9, element 902, and col. 12, lines 63-67].

Furthermore, Churchill teaches that the output from the programmable non-volatile fuse circuit may be sent to a multiplexor prior to being used to configure the adjustable delay element [FIG. 11B, elements 1117 and 1119, and col. 14, lines 15-25]. However, Churchill does not teach that the circuit further comprises a volatile latch coupled between the programmable non-volatile fuse circuit and the adjustable delay element.

Bishop teaches that an adjustable delay element may be controlled by output from configuration latches or multiplexors [FIG. 1, element 110 and 122, and col. 5, lines 7-11].

Bishop therefore teaches a circuit that controls the adjustable delay element, and that such a circuit may comprise either multiplexors, as taught by Churchill, or latches, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ configuration latches, whereby a plurality of delay elements coupled to the volatile latch, comprising propagation paths, a plurality of capacitors selectively coupled to the propagation path selectable in response to the volatile latch, as taught by Bishop. One of ordinary skill in the art would have been motivated to do so that the configuration information from the programmable fuse circuit may be used to control the adjustable delay element.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of using a programmable delay system to adjust the timing of memory control signals. Moreover, the latch means taught by Bishop would improve the flexibility of Churchill because it allowed the configuration to be maintained to the adjustable delay circuit even if the fuse circuit were subsequently re-programmed.

16. As to claims 7 and 14, Churchill discloses the adjustable delay element comprises a plurality of capacitors selectively coupled to a propagation path [col. 13, lines 41-45]. When combined with the configuration latch taught by Bishop, said plurality of capacitors is selectively activated by the volatile latch circuit, substantially as claimed.

17. As to claim 8, Bishop discloses the circuit further comprises logic circuitry coupled to an input of the plurality of adjustable delay elements [FIG. 1, element 110 and 122, and col. 5, lines 7-11], and latch circuitry coupled to an output of the plurality of adjustable delay elements [FIG. 1, element 114].

18. As to claim 13, Churchill and Bishop disclose the adjustable timing circuit comprising a programmable non-volatile fuse circuit that controls an adjustable delay element via a volatile latch circuit, substantially as claimed. Churchill further teaches that the adjustable timing circuit may be used to control access to an array of SRAM memory cells [col. 4, lines 6-30]. Therefore, Churchill and Bishop teach a synchronous memory device comprising both the memory and the adjustable timing circuit, substantially as claimed.

19. As to claim 19, Churchill and Bishop disclose the adjustable timing circuit comprising a programmable non-volatile fuse circuit that controls an adjustable delay element via volatile latches, substantially as claimed. Because Churchill and Bishop teach the circuit, Churchill and Bishop also teach the method implemented by the circuit, substantially as claimed.

20. As to claim 20, Churchill discloses the adjustable delay element comprises a plurality of capacitors selectively coupled to a propagation path [col. 13, lines 41-45].

21. As to claim 21, Churchill discloses the programmable non-volatile fuse circuit comprises a plurality of floating gate transistors [col. 14, lines 44-49]. Churchill teaches that the

programmable element may comprise any type of programmable element, such as an electrical fuse comprising a floating gate transistor.

22. As to claims 22 and 24, Churchill and Bishop disclose the method of using an adjustable timing circuit comprising a programmable non-volatile fuse circuit that controls an adjustable delay element via volatile latches, substantially as claimed. Churchill further teaches that the adjustable timing circuit may be used to test a memory system [col. 3, lines 21-37]. Because Churchill teaches the method, Churchill also teaches the method to test a memory system implementing said method, substantially as claimed.

In addition, Churchill teaches how the timing of the memory signals may be monitored and stored in a scan register memory, and that the adjustable timing circuit may be subsequently reprogrammed in response to the results in order to improve the timing of the memory system [col. 3, 48-61]. Churchill therefore teaches using a sequential process of programming a propagation path delay time, testing the results, and adjusting the propagation path delay time thereafter, substantially as claimed.

23. As to claim 23, Churchill discloses the programmable non-volatile fuse circuit comprises a plurality of floating gate transistors [col. 14, lines 44-49]. Churchill teaches that the programmable element may comprise any type of programmable element, such as an electrical fuse comprising a floating gate transistor. Churchill also teaches that the method may be used to test access to synchronous memory [col. 3, lines 21-37], such as a flash memory, substantially as claimed.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ec
May 29, 2003

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100